REMARKS

The specification has been revised to clarify/correct the grammar and to correct various self-evident errors in punctuation, reference-symbol usage, figure identification, and singular-versus-plural case. In addition, the word "laterally" has been inserted in two instances in paragraphs 10 and 21 of the specification to verbally clarify the geometry as illustrated in the drawings

The citation information for the journal references cited in paragraphs 15, 18, and 19 of the specification has been corrected. Since underlining is used to indicate inserted material in the revisions to the specification, the underlining of the names of the journals in the journal references cited in those three paragraphs has been changed to present the journal names in italics.

In paragraph 44 of the specification, the brief description of Fig. 10 has been revised to conform to what is shown in Fig. 10. References to "threshold voltage" in paragraphs 119 and 124 have been revised to appropriately use the "V_{T0}" threshold-voltage symbol in conformity with what is shown in Fig. 8.

A missing percent sign (%) has been inserted in paragraph 181 of the specification. Polysilicon "layer" in the next-to-last sentence in paragraph 211 has been corrected to polysilicon "spacer" so as to conform with the use of polysilicon "spacer" in the immediately previous sentence in paragraph 211.

The first sentences in paragraphs 238 and 241 of the specification present total dosages of the HV source/drain extension dopants and then indicate that those dosages are suitable "regardless of the number M_A of azimuthal angles". The second sentence in each of paragraphs 238 and 241 then provides that one fourth of the each source/drain extension dosage is preferably furnished at each azimuthal angle. Since this situation necessarily arises when there are four azimuthal angles, the second sentence in each of paragraphs 238 and 241 has been amended to specify that the conditions recited in that sentence apply to "the preferred case where M_A is 4".

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Finally, the specification uses the expression "very heavily doped" to indicate dopant levels corresponding to double-plus (++) signs. Inasmuch as gate electrode 122 of insulated-gate field-effect transistor 104 is illustrated in the drawings as being doped to a value in the "++" regime, "heavy dosage" and "heavily doped" as used in paragraph 253 of the

specification in connection with gate electrode 122 have been respectively changed to "very heavy dosage" and "very heavily doped" in order to conform with the drawings and the earlier material disclosed in the specification.

Claims 1, 5, 6, 8, 12, 16 - 19, 23, 31, 38, 39, and 41 have been amended. Claim 3 has been canceled for the reasons discussed below. Claims 43 - 80 have been canceled as a result of the election of Claims 1 - 42 in response to the Restriction Requirement mailed 2 September 2005.

Claims 81 - 105 have been added to claim the invention with more particularity. New Claim 94 is an independent claim. The reminder of the new claims are dependent claims. Accordingly, Claims 1, 2, 4 - 42, and 81 - 105 are now pending.

Claims 1, 2, and 5 - 7 have been rejected under 35 USC 102(b) as anticipated by Pfiester, U.S. Patent 5,536,962. Claims 3 and 4 have been rejected under 35 USC 103(a) as obvious based on Pfiester. These rejections are respectfully traversed in view of the revisions made to the claims.

Pfiester discloses a semiconductor structure containing n-channel "buried channel" driver insulated-gate field-effect transistor ("IGFET") 16 and n-channel surface-channel pass IGFET 28 which share common n-type drain region 52/63/54 consisting of main portion 52 and more lightly doped lateral extensions 63 and 54. Main drain portion 52 and lateral extension 63 form the active drain for buried-channel IGFET 16. Main drain portion 52 and lateral extension 54 form the active drain for surface-channel IGFET 28

Buried-channel driver IGFET 16 further includes n-type source region 62/64, n-type channel surface layer 60 extending between source/drain regions 62/64 and 52/63/54, p-type "buried channel" region 56 extending between source/drain regions 62/64 and 52/63/54 below channel surface layer 60, gate dielectric layer 58 situated on channel surface layer 60, and gate electrode 40 formed with p-type polycrystalline silicon ("polysilicon") layer 74 and overlying tungsten silicide layer 76. Source region 62/64 is formed with main portion 62 and more lightly doped lateral extension 64.

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Surface-channel pass IGFET 28 further includes n-type source region 50/53, p-type channel region 46 extending between source/drain regions 50/53 and 52/63/54, gate dielectric layer 48 situated on channel region 46, and gate electrode 44 formed with n-type polysilicon

layer 68 and overlying tungsten silicide layer 70. Source region 50/53 is formed with main portion 50 and more lightly doped lateral extension 53.

As disclosed in cols. 4 and 5 of Pfiester, gate dielectric layer 58 for buried-channel IGFET 16 is formed at the same time as gate dielectric layer 48 for surface-channel IGFET 28. In particular, a silicon oxide layer is first thermally grown along upper surface 66 of doped monocrystalline silicon ("monosilicon") substrate 11. Although Pfiester does not mention the conductivity type of the monosilicon used in forming the silicon oxide layer, this monosilicon would appear to be p type in order to have the requisite pn junctions along source/drain regions 62/64, 50/53, and 52/63/54.

A thin layer of polysilicon is deposited on the silicon oxide layer. P-type and n-type dopants are selectively ion implanted through the polysilicon and silicon oxide and into substrate 11 to define p-type channel region 46, p-type buried channel region 56, and n-type channel surface layer 60. Gate electrode 40 for buried-channel IGFET 16 and gate electrode 44 for surface-channel IGFET 28 are formed according to a procedure in which additional polysilicon is apparently deposited on the first-mentioned polysilicon. The silicon oxide directly underlying gate electrode 40 constitutes gate dielectric layer 58 for buried-channel IGFET 16. The silicon oxide directly underlying gate electrode 44 similarly constitutes gate dielectric layer 58 for surface-channel IGFET 28.

Independent Claim 1 has been amended to include the further limitation of dependent Claim 3, now canceled, subject to the additional restriction that the gate dielectric layer of the n-channel channel-junction IGFET be "materially" thicker than the gate dielectric layer of the n-channel surface-channel IGFET. As amended, Claim 1 thus recites:

1. A structure comprising:

an n-channel surface-channel insulated-gate field-effect transistor ("SCIGFET") comprising a pair of laterally separated n-type source/drain zones situated in a semiconductor body along a major surface thereof, a p-type channel zone situated between the n-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the n-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel SCIGFET from its source/drain and channel zones; and

a normally off n-channel channel-junction insulated-gate field-effect transistor ("CJIGFET") comprising a pair of laterally separated n-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the n-channel CJIGFET's

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source/drain zones in the semiconductor body along its major surface and more lightly doped than the n-channel CJIGFET's source/drain zones, a gate electrode situated over the channel zone of the n-channel CJIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel CJIGFET from its source/drain and channel zones, the gate dielectric layer of the n-channel CJIGFET being materially thicker than the gate dielectric layer of the n-channel SCIGFET.

With respect to Claim 1, the Examiner states on page 2 of the Office Action that:

> Pfiester 5,536,962 teaches all the claimed invention including structure comprising a surface channel MOS transistor and a buried channel MOS transistor and associated components of gate 68, source/drain50/52/53/54, and channel 46 for the n channel surface channel MOS 28 and the normally off n channel channel junction IGFET 16 and associated components of gate 74, source/drain 52/62/63/64, channel 60.

In regard to Claims 3 and 4, the Examiner asserts on pages 3 and 4 of the Office Action that:

> Although Pfiester as applied above does not recite the thicker gate dielectric as in claim 3 and the greater channel length, in claim 4, for the surface channel transistor, such would have been obvious and would have been encompassed in Pfiester for the following reasons. Initially, the difference in thickness or channel length is not sufficiently defined to impart patentability, there being no definite demarcation between the respective dimensions as to how much thicker or how much greater, respectively, thus does not distinguish over normal variance in devices and since there are only three possible alternatives, namely being identical dimension thickness or channel length, or either thicker or thinner, or either greater or smaller, and the selection of one out of these two or three possibilities would have been obvious, and given that Pfiester is not required the gate dielectric to be of identical thickness and also does not reuire [sic, require] identical channel lengths. Additionally, such selection of particular dimensions would permit one skilled in the art to optimize the characteristics of the transistors in question and would have been within a matter of routine optimization.

Normal fabrication process variances can, of course, cause two dielectric layers formed at the same time and along largely the same material, e.g., silicon doped with a particular dopant species, to differ slightly in thickness. In fact, the thickness of each dielectric layer will invariably differ slightly from point to point along that dielectric layer. However, the requirement of canceled dependent Claim 3 that the gate dielectric layer of the n-channel CJIGFET be thicker than the gate dielectric layer of the n-channel SCIGFET was intended to apply to situations <u>beyond</u> the slight thickness differences arising from normal fabrication process variances. In order to make this distinction clear in amending Claim 1 to

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include the further limitation of Claim 3, Claim 1 has been further amended to require that that the gate dielectric layer of the channel-junction IGFET be "materially" thicker than the gate dielectric layer of the surface-channel IGFET. The word "materially" requires that the difference between the (average) gate dielectric thicknesses be greater than what would occur with normal fabrication variances.

Gate dielectric layers 58 and 48 in Pfiester contain portions of the silicon oxide layer thermally grown along upper silicon surface 66 from the material of substrate 11. As indicated below, these silicon oxide portions respectively constitute intermediate portions of dielectric layers 58 and 48 in Pfiester's final device structure. The intermediate portions of dielectric layers 58 and 48 are grown from p-type monosilicon. Accordingly, the intermediate silicon oxide portions are of largely the same average thickness. During subsequent thermal processing, the silicon adjacent to each of the two silicon oxide portions appears to be subjected to largely the same heating conditions as the silicon adjacent to the other silicon oxide portion. To a first approximation, dielectric layers 58 and 48 should therefore be of approximately the same average thickness. Fig. 3 of Pfiester illustrates dielectric layers 58 and 48 as being of the same thickness.

One of gate dielectric layers 58 and 48 can actually be thicker than the other due to additional factors such as the crystal structure, dopant types, dopant concentrations, defect types, and defect densities in the silicon from which dielectric layers 58 and 48 are grown. The information given in Pfiester is insufficient to determine the quantitative effect of these additional factors on the average thickness of each of dielectric layers 58 and 48. However, Pfiester states in the middle of col. 5 that:

> It is known that n-type polycrystalline silicon oxidizes more rapidly than p-type polysilicon. The differential oxidation rate of n-type and p-type polycrystalline silicon advantageously assists in providing a greater current gain in the driver transistor 16 relative to pass transistor 28. This is because more lateral oxidation takes place at the interface between n-type polycrystalline silicon layer 68 and gate dielectric layer 48, than at the corresponding interface between p-type polycrystalline layer 74 and gate dielectric layer 58. The enhanced "bird's beak" under polycrystalline silicon layer 68 (not shown) slightly reduces the current gain in pass transistor 28.

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As the preceding material indicates, gate dielectric layer 58 of buried-channel driver IGFET 16 includes an upper silicon oxide portion grown from the p-type material of polysilicon layer 74. Gate dielectric layer 48 of surface-channel pass IGFET 28 similarly includes an

upper silicon oxide portion grown from the n-type material of polysilicon layer 68. Since n-type polysilicon oxidizes more rapidly than p-type polysilicon, the upper portion of dielectric layer 48 of surface-channel IGFET 28 is of greater average thickness than the upper portion of dielectric layer 58 of buried-channel IGFET 16.

Pfiester introduces p-type and n-type dopants into substrate 11 to form p-type channel region 46 and n-type channel surface layer 60 subsequent to growing the above-mentioned oxide layer along upper silicon surface 66. Thermal steps are performed on Pfiester's device structure subsequent to forming channel region 46 and channel surface layer 60. Hence, gate dielectric layer 58 of buried-channel driver IGFET 16 also includes a lower silicon oxide portion grown from the n-type monosilicon of surface layer 60 while gate dielectric layer 48 of surface-channel pass IGFET 28 includes a lower silicon oxide portion grown from the p-type monosilicon of channel region 46. The thickness of dielectric layer 58 of buried-channel IGFET 16 thereby consists of (a) a lower portion arising from silicon oxide grown from the n-type monosilicon of channel surface layer 60, (b), an intermediate portion arising from the initial thermal growth of the silicon oxide layer from p-type monosilicon of substrate 11, and (c) an upper portion arising from the silicon oxide grown from the p-type polysilicon of polysilicon layer 74. The thickness of dielectric layer 48 of surface-channel IGFET 28 similarly consists of (a) a lower portion arising from silicon oxide grown from the p-type monosilicon of channel region 46, (b), an intermediate portion arising from the initial thermal growth of the silicon oxide layer from p-type monosilicon of substrate 11, and (c) an upper portion arising from the silicon oxide grown from the n-type polysilicon of polysilicon layer 68.

Doped polysilicon thermally oxidizes considerably more rapidly than equivalently doped monosilicon subjected to the same heating conditions. In view of this and the fact that n-type polysilicon oxidizes more rapidly than p-type polysilicon, the amount by which the upper thickness portion of gate dielectric layer 44 averagely exceeds the upper thickness portion of gate dielectric layer 40 would be expected to be greater than the amount, if any, by which the lower thickness portion of dielectric layer 40 averagely exceeds the lower thickness portion of dielectric layer 44. Because the intermediate thickness portions of dielectric layers 40 and 40 are of largely the same average thickness, dielectric layer 48 of surface-channel pass IGFET 28 would be expected to be of somewhat greater average thickness than dielectric layer 44 of buried-channel driver IGFET 16. Pfiester does not meet

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the requirement of canceled Claim 3 that the gate dielectric layer of the n-channel channel-junction IGFET be thicker than the gate dielectric layer of the n-channel surface-channel IGFET. Consequently, Pfiester does not meet the requirement of Claim 1 that the gate dielectric layer of the channel-junction IGFET be materially thicker than the gate dielectric layer of the surface-channel IGFET.

With respect to the Examiner's assertion in regard to Claim 3 that "since there are only three possible alternatives, namely being identical dimension thickness . . ., or either thicker or thinner, . . . and the selection of one out of these two or three possibilities would have been obvious, and given that Pfiester is not required the gate dielectric to be of identical thickness" and that "such selection of particular dimensions would permit one skilled in the art to optimize the characteristics of the transistors in question and would have been within a matter of routine optimization", Pfiester's device structure is designed to enable buried-channel driver IGFET 16 to have higher current gain than surface-channel pass IGFET 28 as, for example, stated in the first paragraph of col. 4. In accordance with what Pfiester states in the above-quoted material from the middle paragraph of col. 5, it appears that this design objective would be at least partially <u>defeated</u> if gate dielectric layer 44 of buried-channel driver IGFET 16 were of greater average thickness than gate dielectric layer 48 of surface-channel pass IGFET 28. A person skilled in the art would thus have <u>no</u> motivation for modifying Pfiester's structure so that dielectric layer 44 of buried-channel IGFET 16 is of greater average thickness than dielectric layer 48 of surface-channel IGFET 28 and, in fact, would have great motivation for <u>avoiding</u> such a modification.

For the same reasons, it would <u>not</u> have been a matter of routine optimization to modify Pfiester's device structure to enable gate dielectric layer 44 of buried-channel driver IGFET 16 to be of greater average thickness than gate dielectric layer 48 of surface-channel pass IGFET 28. Rather than optimizing Pfiester's structure, such a modification would take Pfiester's structure <u>away</u> from the optimum design point. Consequently, Pfiester does not make Claim 1 obvious. Claim 1 is therefore patentable over Pfiester.

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Wang, U.S. Patent 6,621,125 B1, has been made of record by the Examiner but has not been applied against any of the claims. Somewhat similar to Pfiester, Wang discloses a semiconductor structure containing an n-channel buried-channel IGFET and an n-channel surface-channel IGFET. See Fig. 3C of Wang. N-type drain region 88 and n-type source region 90 of the n-channel buried-channel IGFET are separated by more lightly doped n-type

channel region 92. A gate dielectric layer (unlabeled) is situated between p-type polysilicon gate electrode 70 and channel region 92. N-type drain region 84 and n-type source region 86 of the n-channel surface-channel IGFET are separated by a channel portion of p-type substrate 54. A gate dielectric layer (likewise unlabeled) is situated between n-type polysilicon gate electrode 74 and the channel portion of substrate 54.

Fig. 3C of Wang illustrates the gate dielectric layers of the two n-channel IGFETs as being of the same thickness. In cols. 4 and 5, Wang discloses that n-type channel region 92 of the n-channel buried-channel IGFET is created after gate electrodes 70 and 74 are formed. Since gate electrode 70 of the n-chanel buried-channel IGFET consists of p-type polysilicon while gate electrode 74 of the n-channel surface-channel IGFET consists of n-type polysilicon, Claim 1 patentably distinguishes Wang for reasons similar to those which make Claim 1 patentable over Pfiester.

Claims 2 and 4 - 7 all depend (directly or indirectly) from Claim 1. Hence, dependent Claims 2 and 4 - 7 are patentable over Pfiester for the same reasons as Claim 1. Claims 2 and 4 - 7 also patentably distinguish Wang for the same reasons as Claim 1.

In regard to Claims 5 and 6, the Examiner asserts on pages 2 and 3 of the Office Action that:

> Regarding the current conduction in claims 5 and 6, these do not require or recite any additional structure but only mode of operation and does not impart patentability over the disclosed structure which presumably would be capable to so perform given the same structures are taught. A recitation directed to the manner in which a claimed apparatus is intended to be used does not distinguish the claimed apparatus from the prior art — if the prior art has the capability to so perform. See MPEP 2114 and Ex parte Masham, 2 USPQ2d 1647 (1987). The recitation of a new intended use for an old product does not make a claim to that old product patentable. In re Schreiber, 44 USPQ2d 1429 (Fed. Cir. 1997)

Claims 5 and 6 have been amended to add structural requirements to the specified current conduction limitations. As amended, Claims 5 and 6 recite:

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> 5. A structure as in Claim 1 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct current through a field-induced surface channel that extends across the channel zone of the n-channel CJIGFET substantially up to its gate dielectric layer.
>
> 6. A structure as in Claim 1 wherein the n-channel CJIGFET is of dimensions and dopant concentrations so as to conduct current through a

metallurgical subsurface channel that extends across the channel zone of the n-channel CJIGFET below, and spaced apart from, its gate dielectric layer.

The dimensions and dopant concentrations of a channel-junction IGFET determine whether it conducts current through a field-induced surface channel or a metallurgical subsurface channel. Hence, the revisions of Claims 5 and 6 to refer to the dimensions and dopant concentrations of the channel-junction IGFET in the preceding way add structural requirements to the respective surface and subsurface current conduction limitations.

Pfiester does not disclose whether buried-channel IGFET 16 conducts current through a subsurface metallurgical channel or a field-induced surface channel. However, the above application discloses that long-channel threshold voltage V_{T0} for an n-channel channel-junction IGFET at a given gate dielectric thickness and a given set of dopant concentrations is greater for conduction via a field-induced surface channel than via a metallurgical subsurface channel. In particular, application Fig. 8 indicates that a normally off n-channel CJIGFET cannot operate with a field-induced channel at a V_{T0} value of 0.9 V when net body-material dopant concentration N_B is 3×10^{16} atoms/cm^3, net gate-electrode polysilicon dopant concentration N_{POLY} is 1×10^{20} atoms/cm^3, gate-dielectric thickness t_{GD} is 10 nm, and channel-zone dopant concentration N_C varies from a low value as little as 1×10^{16} atoms/cm^3 to a high value at least as high as 5×10^{17} atoms/cm^3. Instead, threshold voltage V_{T0} must be 1.0 V or higher for operation with a field-induced surface channel.

In the last full paragraph of col. 4, Pfiester discloses that the threshold voltages of the pass and driver IGFETs is controlled to be within the range of 0.7 V to 1.0 V. Since it is difficult to operate with a field-induced surface channel at a V_{T0} value below 1.0 V for typical gate-dielectric thicknesses and dopant concentrations, it is a reasonable inference that buried-channel IGFET 16 would be expected to operate with a subsurface metallurgical channel. This inference is strongly supported by Pfiester's description of IGFET 16 as a "buried channel" device and the absence of any recognition in Pfiester that an n-channel IGFET having an n-type channel zone doped more lightly than the IGFET's n-type source/drain zones can operate with a field-induced surface channel for certain dimension and dopant-concentrations conditions. The requirement of Claim 5 that the n-channel CJIGFET be " of dimensions and dopant concentrations so as to conduct current through a field-induced surface channel" thereby further distinguishes Pfiester and establishes a separate basis for allowing Claim 5 over Pfiester.

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The n-channel buried-channel IGFET in Fig. 3C of Wang is configured the same as the n-channel buried-channel IGFET in Fig. 2A of Wang. In the last paragraph in col. 3, Wang discloses that the n-channel buried-channel IGFET in Fig. 2A conducts current through a path away from the gate oxide layer, i.e., through a metallurgical subsurface channel. Accordingly, the field-induced subsurface channel limitation of Claim 5 also further distinguish Wang.

Claims 8 - 42 have been indicated as being allowable if rewritten in independent form. Claims 8 - 42 all depend (directly or indirectly) from Claim 1. Since Claim 1 is now patentable over Pfiester and patentably distinguishes Wang, dependent Claims 8 - 42 are allowable in their current form.

Note that Claims 16, 18, 38, and 39 have been revised in a similar manner to Claims 5 and 6 to add structural requirements to the specified current conduction limitations. Claims 12, 17, and 19 have been revised to conform to the revisions to Claim 1. The adverb "materially" has been inserted before "thicker" in each of Claims 12, 17, 19, and 31 for the same reasons that "materially" has been inserted before "thicker" in Claim 1. Claims 23 and 41 have been amended to make it clear that the recited "channel zone" means the channel zone of the n-channel CJIGFET.

New Claims 81 - 93 all depend (directly or indirectly) from Claim 1. Hence, dependent Claims 81 - 93 are patentable over Pfiester and patentably distinguish Wang for the same reasons as Claim 1.

In addition, Claim 81 provides that "the gate dielectric layer of the n-channel CJIGFET is at least twice as thick as the gate dielectric layer of the n-channel SCIGFET". Claims 84, 87, 89, and 91 recite minimum two-fold thickness limitations similar to that of Claim 81. The minimum two-fold thickness further limitations of Claims 81, 84, 87, 89, and 91 are supported at paragraph 93 of the specification.

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Neither Pfiester nor Wang discloses or in any way suggests the minimum two-fold thickness limitation of any of Claims 81, 84, 87, 89, and 91. Accordingly, Claims 81, 84, 87, 89, and 91 are separately patentable over Pfiester and further patentably distinguish Wang.

Claim 82 recites that the claimed structure includes "circuitry for providing voltages to the n-channel CJIGFET and the n-channel SCIGFET and for operating the n-channel CJIGFET across a materially greater voltage range than the n-channel SCIGFET". Claims

85, 88, 90, and 92 recite voltage-range limitations similar to that of Claim 83. The voltage-range further limitations of Claims 82, 85, 88, 90, and 92 are supported at paragraphs 26, 54, 59, 61, and 92 of the specification.

Neither Pfiester nor Wang discloses or suggests the voltage-range limitation of any of Claims 82, 85, 88, 90, and 92. Hence, Claims 82, 85, 88, 90, and 92 are separately patentable over Pfiester and further patentably distinguish Wang.

Claim 83 specifies that the voltage-providing/operating circuitry comprises (a) analog circuitry for providing voltages to the n-channel CJIGFET and (b) digital circuitry for providing voltages to the n-channel SCIGFET. Claims 86 and 93 recite analog/digital lilmitations similar to that of Claim 83. The analog/digital further limitations of Claims 83, 86, and 93 are supported at paragraphs 33, 54, and 69 of the specification.

Neither Pfiester nor Wang discloses or suggests the analog/digital limitation of any of Claims 83, 86, and 93. As a result, Claims 83, 86, and 93 are separately patentable over Pfiester and further patentably distinguish Wang.

New independent Claim 94 constitutes dependent Claim 5 rewritten in independent form as it depended from the original version of Claim 1 subject to structural requirements being added to the specified current conduction limitations as in the amended version of Claim 5. Accordingly, Claim 94 recites:

94. A structure comprising:

an n-channel surface-channel insulated-gate field-effect transistor ("SCIGFET") comprising a pair of laterally separated n-type source/drain zones situated in a semiconductor body along a major surface thereof, a p-type channel zone situated between the n-channel SCIGFET's source/drain zones in the semiconductor body along its major surface, a gate electrode situated over the channel zone of the n-channel SCIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel SCIGFET from its source/drain and channel zones; and

a normally off n-channel channel-junction insulated-gate field-effect transistor ("CJIGFET") comprising a pair of laterally separated n-type source/drain zones situated in the semiconductor body along its major surface, an n-type channel zone extending between the n-channel CJIGFET's source/drain zones in the semiconductor body along its major surface and more lightly doped than the n-channel CJIGFET's source/drain zones, a gate electrode situated over the channel zone of the n-channel CJIGFET and extending partially over its source/drain zones, and a gate dielectric layer separating the gate electrode of the n-channel CJIGFET from its source/drain

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and channel zones, the n-channel CJIGFET being of dimensions and dopant concentrations so as to conduct current through a field-induced surface channel that extends across the channel zone of the n-channel CJIGFET substantially up to its gate dielectric layer.

Claim 94 is patentable over Pfiester for the above-mentioned reasons that Claim 5 is separately patentable over Pfiester. Similarly, Claim 94 patentably distinguishes Wang for the above-mentioned reasons that Claim 5 further patentably distinguishes Wang.

Claims 95 - 105 all depend (directly or indirectly) from Claim 94. Dependent Claims 95 - 105 are therefore patentable over Pfiester and patentably distinguish Wang for the same reasons as Claim 94.

Claims 96, 97, 100, 101, 104, and 105 respectively repeat the voltage-range and analog/digital further limitations of Claims 82, 83, 85, 86, 92, and 93. Consequently, Claims 96, 97, 100, 101, 104, and 105 are separately patentable over Pfiester and further patentably distinguish Wang for the same respective reasons as Claims 82, 83, 85, 86, 92, and 93.

In short, Claims 1, 2, 4 - 7, and 81 - 105 have been shown to be patentable over Pfiester and to patentably distinguish Wang. Claims 8 - 42 are allowable in their current form. Accordingly, Claims 1, 2, 4 - 42, and 81 - 105 should be allowed so that the application may proceed to issue.

Please telephone Applicants' Attorney at 650-964-9767 if there are any questions.

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